INTERNAL VOLTAGE GENERATING CIRCUIT IN SEMICONDUCTOR MEMORY DEVICE

Field of the Invention

The present invention relates to a semiconductor memory device; and, more particularly, to an internal voltage generating circuit in the semiconductor memory device.

Description of Related Art

Generally, as a semiconductor chip is highly integrated, a cell size becomes smaller and an operation voltage is also decreased. Most of semiconductor chip has an internal voltage generator for generating an internal voltage necessary for an operation of an internal circuit in the semiconductor chip. It is an important factor that the internal voltage having a stable voltage level is constantly provided.

Fig. 1 is a circuit diagram illustrating a conventional internal voltage generating circuit of a semiconductor memory device.

As shown, the internal voltage generating circuit includes a comparator 10 for comparing a voltage level of an internal voltage Vint and a reference voltage VREF, and a pull-up PMOS transistor PM1 which is connected between a power supply voltage VDD and an output terminal and whose gate receives an output signal drv_onb of the comparator 10. It is

preferred that the comparator 10 is configured with a typical differential amplifier of a current mirror type.

The output signal drv_onb of a logic low level is outputted from the comparator 10 when the internal voltage Vint is lower than the reference voltage VREF by comparing the reference voltage VREF with the internal voltage Vint., so that the pull-up PMOS transistor MP1 is turned on. Therefore, the voltage level of the internal voltage Vint is increased.

On the other hand, if the voltage level of the internal voltage level Vint is increased higher than the voltage level of the reference voltage VREF, the output signal drv_onb of the comparator 10 becomes a logic high level, so that the pull-up PMOS transistor MP1 is turned off. Therefore, a rising of the voltage level of the internal voltage Vint is stopped.

The internal voltage generated from the internal voltage generating circuit is used as a source follower of the internal circuit 100. The above comparing procedure is repeated until the voltage level of the internal voltage Vint becomes the same voltage level of the reference voltage VREF after power consumption is generated by operating the internal circuit.

The power consumption of the internal circuit is increased as the semiconductor device is manufactured to have a high operation speed. Therefore, a size of a driver, i.e., the pull-up PMOS transistor MP1, in the internal voltage generating circuit should be increased to generate a stable

internal voltage Vint. Also, as the operation voltage is decreased, a threshold voltage of a MOS transistor is gradually decreased.

Accordingly, there is problem that the internal voltage Vint is increased in proportion to increase of the power supply voltage VDD by a sub-threshold current produced in the pull-up PMOS transistor MP1.

Generally, the sub-threshold current (Isub) flowing in the MOS transistor is defined as a following equation 1:

$$Isub = I_o \cdot \exp[q \cdot Vgs/nkT] \qquad \text{Eq.1}$$

$$I_o = Isub_o(W/L)$$

Where q, Vgs, k and T represent a charge of an electron, a gate-source voltage, a temperature constant and an absolute temperature, respectively. Also, Isubo is a current value obtained in a process and W and L represent a width and a length of the MOS transistor.

As shown in Eq.1, the sub-threshold current is linearly proportional to the width of the MOS transistor and is exponentially proportional to the Vgs.

Summary of the Invention

It is, therefore, an object of the present invention to provide an internal voltage generating circuit in a semiconductor memory device capable of suppressing a potential

increase of an internal voltage due to a sub-threshold current flowing in a pull-up driver.

In accordance with an aspect of the present invention, there is provided an internal voltage generating circuit in a semiconductor memory device including: a comparing unit for comparing a voltage level of an internal voltage with that of a reference voltage; a pull-up driving unit for performing a pull-up operation for an output terminal in response to an output signal of the comparing unit; and a discharging unit for discharging the output terminal in a period of which the voltage level of the internal voltage is higher than a predetermined target voltage level.

In accordance with another aspect of the present invention, there is provided an internal voltage generating circuit in a semiconductor memory device, including: a comparing unit for comparing a voltage level of an internal voltage with that of a reference voltage; a pull-up driving unit for performing a pull-up operation for an output terminal in response to an output signal of the comparing unit; and a first discharging unit for discharging the output terminal when the voltage level of the internal voltage is higher than a predetermined target voltage level in response to the internal voltage.

Brief Description of the Drawings

The above and other objects and features of the instant

invention will become apparent from the following description of preferred embodiments taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a circuit diagram illustrating a conventional internal voltage generating circuit of a semiconductor memory device;

Fig. 2 is a circuit diagram illustrating an internal voltage generating circuit in accordance with the present invention; and

Fig. 3 is a graph showing simulation results of the internal voltage of the internal voltage generating circuit in Figs. 1 and 2.

Detailed Description of the Invention

Hereinafter, an internal voltage generating circuit in a semiconductor memory device according to the present invention will be described in detail referring to the accompanying drawings.

Fig. 2 is a circuit diagram illustrating an internal voltage generating circuit in accordance with the present invention.

The internal voltage generating circuit includes a comparator 20 for comparing a voltage level of an internal voltage level Vint and a reference voltage VREF, a pull-up PMOS transistor MP2 which is connected between a power supply voltage VDD and an output terminal and whose gate receives an

output signal drv_onb of the comparator 20, and discharge units 30, 40 and 50 for discharging the output terminal at a period that a voltage level of the internal voltage Vint is higher than a predetermined target voltage level. Herein, it is preferable that the comparator 20 is configured with a typical differential amplifier of a current mirror type.

A first discharge unit 50 is to discharge the output terminal when the voltage level of the internal voltage Vint and a second discharge unit 30 and 40 is to discharge the output terminal in response to a voltage level of the power supply voltage VDD. The first discharge unit 50 includes a plurality of diode-coupled NMOS transistors MN2, MN3 and MN4, which are connected between the power supply voltage VDD and a ground voltage VSS in series. The second discharge unit includes a voltage divider 30 and a discharge driver 40. The voltage divider 30 generates a discharge control signal Va by dividing the power supply voltage VDD and the discharge driver 40 discharges the output terminal in response to the discharge control signal Va. The voltage divider 30 can be configured with a first resistor R1 and a second resistor R2 connected between the power supply voltage VDD and the ground voltage VSS in series. The discharge driver 40 includes an NMOS transistor MN1 which is connected between the output terminal and the ground voltage VSS and whose gate receives the discharge control signal Va.

Hereinafter, an operation of the internal voltage generating circuit in accordance with the preferred embodiment

of the present invention will be described.

The output signal drv_onb of a logic low level is outputted from the comparator 20 when the internal voltage Vint is lower than the reference voltage VREF by comparing the reference voltage VREF with the internal voltage Vint, so that the pull-up PMOS transistor MP2 is turned on. Therefore, the voltage level of the internal voltage Vint is increased.

On the other hand, if the voltage level of the internal voltage level Vint is increased higher than the voltage level of the reference voltage VREF, the output signal drv_onb of the comparator 20 becomes a logic high level, so that the pull-up PMOS transistor MP2 is turned off. Therefore, a rising of the voltage level of the internal voltage Vint is stopped.

However, the voltage level of the internal voltage Vint is substantially increased due to a sub-threshold current flowing in a state of which the pull-up PMOS transistor MP2 is turned off. At this time, the discharge units 30, 40 and 50 are operated, so that an abnormal rising of the voltage level of the internal voltage Vint can be suppressed.

The diode-coupled NMOS transistor has characteristics that the NMOS transistor is turned on such as a diode when a voltage which is higher than the threshold voltage Vtn of the NMOS transistor is applied to a gate (or drain), and the NMOS transistor is turned off to thereby have an effective resistance corresponding to a threshold voltage when a voltage of blow threshold voltage of the NMOS transistor is applied.

Accordingly, if the plurality of diode-coupled NMOS transistors are connected in series, when the voltage level on the output terminal is higher than n X Vtn, where n represents the number of NMOS transistors, all of NMOS transistors are turned on, so that the output terminal is discharged. On the other hand, if the voltage level of the internal voltage Vint is blow n X Vtn, all of NMOS transistors are turned off, so that a discharge operation from the output terminal is stopped.

Accordingly, if the number of the NMOS transistors or the threshold voltage of the NMOS transistor is adjusted to have that the n X Vtn is higher than the internal voltage level, the rising of the internal voltage Vint can be suppressed with an extra control circuit.

The discharge control signal Va is determined as following equation 2:

$$Va = (R2/(R1+R2)) \times VDD \qquad \text{Eq. 2}$$

Namely, the discharge control signal Va is linearly varied according to voltage level variation of the power supply voltage VDD. The voltage level of the discharge control Va can be controlled by adjusting resistance values of resistors R1 and R2. If the discharge control signal Va is applied to the gate of the NMOS transistor MN1, a discharge operation is performed by turning on the NMOS transistor in a period of which the internal voltage Vint is increased over a

target voltage level. Therefore, abnormal rising of the internal voltage Vint can be suppressed.

After fabricating the semiconductor memory device, the voltage level of the power supply voltage may be increased in a test process such as a burn-in test. At this time, the voltage level of the internal voltage is increased according to a voltage level of the power supply voltage VDD. If the NMOS transistor MN1 is designed to be operated in a saturation region by adjusting the voltage level of the discharge control signal Va, an abnormal rising of the voltage level of the internal voltage Vint can be suppressed.

Also, when the voltage level of the power supply voltage VDD is not varied such as a normal operation, if the discharge control signal Va is adjusted to perform a discharge operation as much as the sub-threshold current measured through a test, the abnormal rising of the voltage level of the internal voltage Vint can be suppressed.

Fig. 3 is a graph showing simulation results of the internal voltage of the internal voltage generating circuit in Figs. 1 and 2.

As shown, the voltage level of the internal voltage Vint_old is increased according to the prior art as the power supply voltage is increased, however, the voltage level of the internal voltage Vint_new is not increased over a target voltage, e.g., 1.6 V, in accordance with the present invention as the power supply voltage VDD is increased.

In the first discharge unit 50, even if three diode-

coupled NMOS transistors are used, the number of the diode-coupled NMOS transistors can be adjusted according to a target voltage level of the internal voltage Vint and a threshold voltage of the NMOS transistor.

Also, in accordance with the preferred embodiment of the present invention of the present invention, two discharge units are used. However, one of discharge units can be used to suppress the abnormal rising of the voltage level of the internal voltage Vint.

As mentioned above, since the abnormal rising of the voltage level of the internal voltage due to the sub-threshold current flowing in the pull-up driver can be suppressed in accordance with the present invention, reliability and an operational characteristic of the semiconductor memory device can be improved.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.